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Application No.: 09/859,659 Attorney Docket No.: EMC2-090PUS

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	John K. Walton	
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Nov 10, 2005
Date of Signature and Transmission

By: [signature]
Richard M. Sharkansky

LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On November 9, 2005, Applicant's attorney received a telephone call from Examiner Lamarre informing Applicant's attorney that there were apparent errors on page 19, line 1 and on page 19 line 21. Applicant's attorney pointed out that the references to the FIGS. should be to FIGS. 9A-20C.

The Examiner called again today, November 10, 2005 and requested a replacement page for page 19.

Attached here is the requested replacement page 19.

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In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

Date November 10, 2005

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Attachment: replacement page 19

connection with FIGS. 9A-20C. Here, each cache memory board includes four memory array regions, an exemplary one thereof being shown and described in connection with FIG. 6 of U. S. Patent No. 5,943,287 entitled "Fault Tolerant Memory System", John K. Walton, inventor, issued August 24, 1999 and assigned to the same assignee as the present invention, the entire subject matter therein being incorporated herein by reference. Further detail of the exemplary one of the cache memory boards.

As shown in FIG. 8A, the board 220_1 includes a plurality of, here four RAM memory arrays, each one of the arrays has a pair of redundant ports, i.e., an A port and a B port. The board itself has sixteen ports; a set of eight A ports M_{A1}-M_{A8} and a set of eight B ports M_{B1}-M_{B8}. Four of the eight A port, here A ports M_{A1}-M_{A4} are coupled to the M_1 port of each of the front-end director boards 190_1, 190_3, 190_5, and 190_7, respectively, as indicated in FIG. 8. Four of the eight B port, here B ports M_{B1}-M_{B4} are coupled to the M_1 port of each of the front-end director boards 190_2, 190_4, 190_6, and 190_8, respectively, as indicated in FIG. 8. The other four of the eight A port, here A ports M_{A5}-M_{A8} are coupled to the M_1 port of each of the back-end director boards 210_1, 210_3, 210_5, and 210_7, respectively, as indicated in FIG. 8. The other four of the eight B port, here B ports M_{B5}-M_{48} are coupled to the M_1 port of each of the back-end director boards 210_2, 210_4, 210_6, and 210_8, respectively, as indicated in FIG. 8

Considering the exemplary four A ports M_{A1}-M_{A4}, each one of the four A ports M_{A1}-M_{A4} can be coupled to the A port of any one of the memory arrays through the logic network 221_{1A}, to be described in more detail in connection with FIGS. 9A-20C. Thus, considering port M_{A1}, such port can be coupled to the A port of the four memory arrays. Likewise, considering the four A ports M_{A5}-M_{A8}, each one of the four A ports M_{A5}-M_{A8} can be coupled to the A port of any one of the memory arrays through the logic network 221_{1B}. Likewise, considering the four B ports M_{B1}-M_{B4}, each one of the four B ports M_{B1}-M_{B4} can be coupled to the B port of any one of the memory arrays through logic network 221_{1B}. Likewise, considering the four B ports M_{B5}-M_{B8}, each one of the four B ports M_{B5}-M_{B8} can be coupled to the B port of any one of the memory arrays through the logic network 221_{2B}. Thus, considering port M_{B1}, such port can be coupled to the B port of the four memory arrays. Thus, there are two paths data and control from either a front-end director 180_1-180_{32} or a back-end director 200_1-200_{32} can reach each one of the four memory arrays on the memory board. Thus, there are eight sets of redundant ports on a memory board, i.e., ports